MBI5152 Application Note

Forward

MBI5152 features an embedded 8k-bit SRAM, which can support up to 1:16 time-multiplexing application. Users only need to send the whole frame data once and to store in the embedded SRAM of LED driver, instead of sending every time when the scan line is changed; therefore it can easily achieve high grayscale with slow DCLK frequency. This article provides the application information of MBI5152, such as the input method of image data and the setting of gray scale data. The detail operations are described in the following sections.

Time-multiplexing Application Design

Figure 1 shows the 3pcs cascaded MBI5152 in 1:16 time multiplexing application.

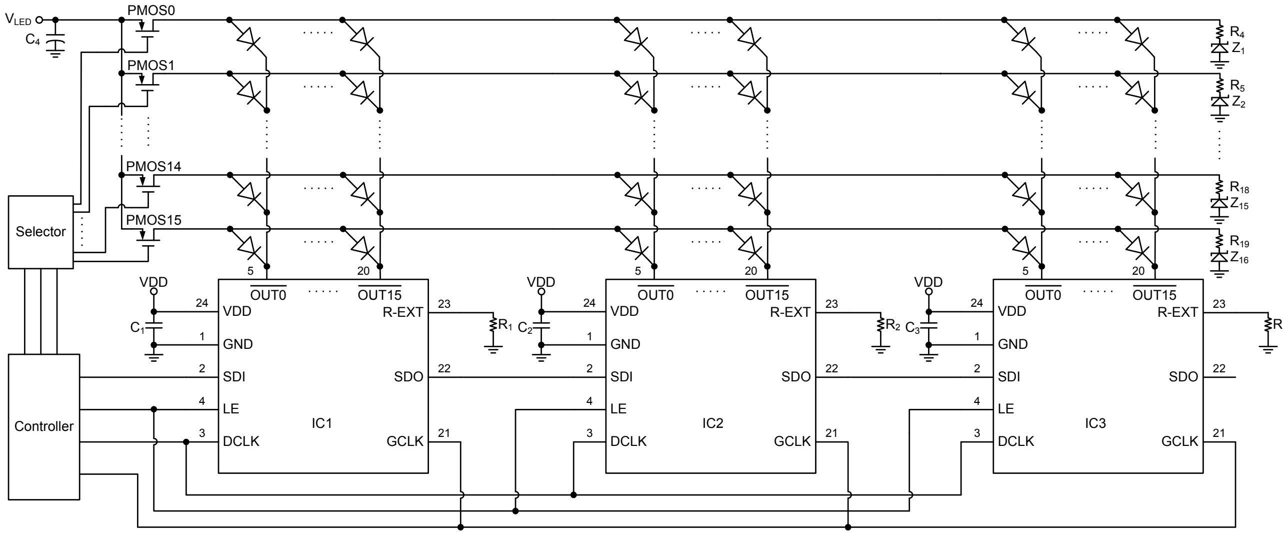

Figure 1. 3pcs cascaded MBI5152 in 1:16 time multiplexing application

Section 1: The Setting of Configuration Register

The setting of configuration data is described as below.

1. The “Pre-Active” command, LE arrested 14-DCLK rising edges, must be announced before “write configuration” command.
2. The data sequence of cascaded IC is ICn→ICn-1→…→IC2→IC1。
3. The sequence of gray scale data is bit15→bit14→…→bit1→bit0。
4. If there are N pcs of MBI5152 in cascaded, then the data length of each “data latch” will be 16 x N bits.
5. When LE is asserted 4-DCLK rising edges, serial data are written to the configuration register 1. When LE is asserted 8-DCLK rising edge, serial data are written to the configuration register 2.
6. The control signals shouldn’t come out until the power of driver board is stable.
7. To ensure the command is valid, the LE false trigger should be avoided in the interval between pre-active and write configuration.

For lower ghost elimination, the configure registers, which are shown in table 1 and 2, are recommended.

Table 1. The recommended configuration register 1 for lower ghost elimination

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	1

Where, bitB~bit0 can be adjusted by display specifications.

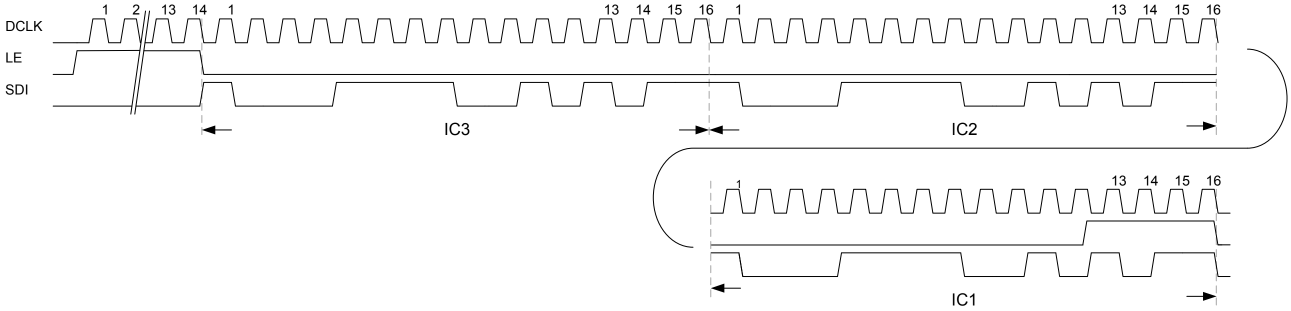

Figure 2. Example of Configuration register 1 setting for 3pcs cascaded MBI5152

Table 2. The recommended configuration register 2 for lower ghost elimination

The setting of configuration register 2 for R-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1

The setting of configuration register 2 for G-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	0	0	0	1	0	1	0	1

The setting of configuration register 2 for B-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	0	0	0	0	0	1	0	1	0	1

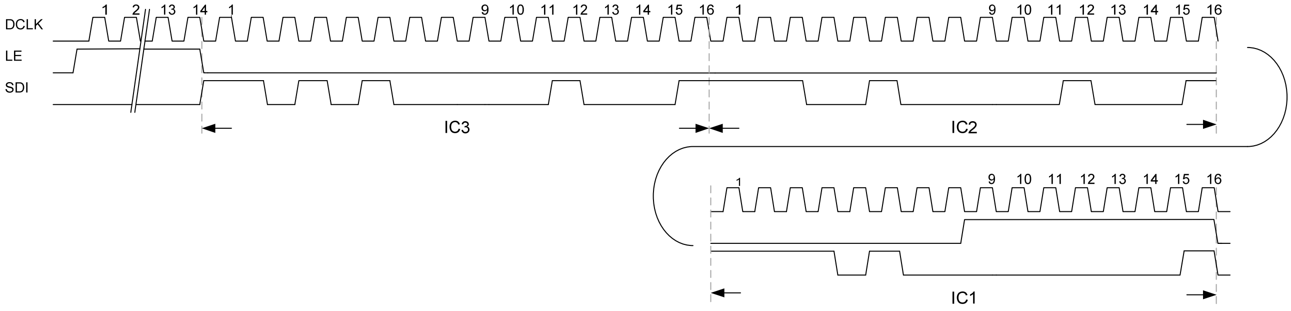

Figure 3. Example of Configuration register 2 setting for 3pcs cascaded MBI5152

Section 2: The Setting of Gray Scale

The setting of gray scale data describes as below.

1. The sequence of input data starts from scan line 1→ scan line 2→…. → scan line M-1→ scan line M (M≦16)
2. The data sequence of cascaded IC is ICn→ICn-1→…. →IC2→IC1.
3. The data sequence of each channel is ch15→ch14→…. →ch0.
4. The data length of each channel is 16-bits, and the default PWM mode is 16-bits. The sequence of gray sacle is bit15→bit14→bit13…→bit0 as figure 4 shows. The 14-bits gray scale can be set through Bit[7]=1 in configuration register 1, and the sequence of gray scale data is bit13→bit12→…→ bit0→ 0→ 0, the last 2-bits (LSB) are set to "0".
5. The frequency of GCLK must be higher than 20% of DCLK to get the correct gray scale data.
6. LE executes the data latch to send gray scale data into SRAM. Each 16xN bits data needs a "data latch command", where N means the number of cascaded driver.
7. After the last data latch, it needs at least 50 GCLKs to read the gray scale data into internal display buffer before the Vsync command comes.
8. Display is updated immediately when MBI5152 receives the Vsync signal.
9. GCLK must keep at low level more than 7ns before MBI5152 receives the Vsync signal.
10. The period of dead time (ie. The 1025th GCLK) must be larger than 100ns.

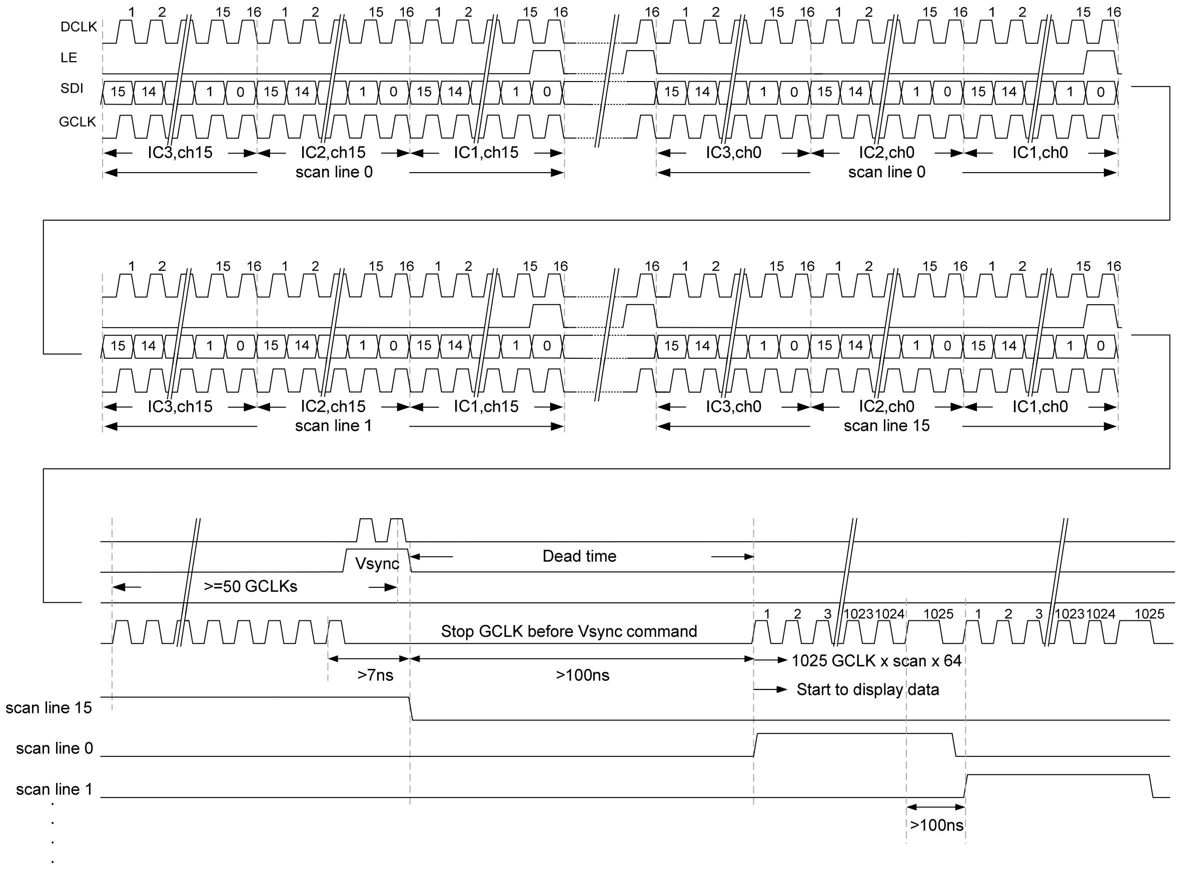

Figure 4. The timing diagram of 16-bit gray scale data

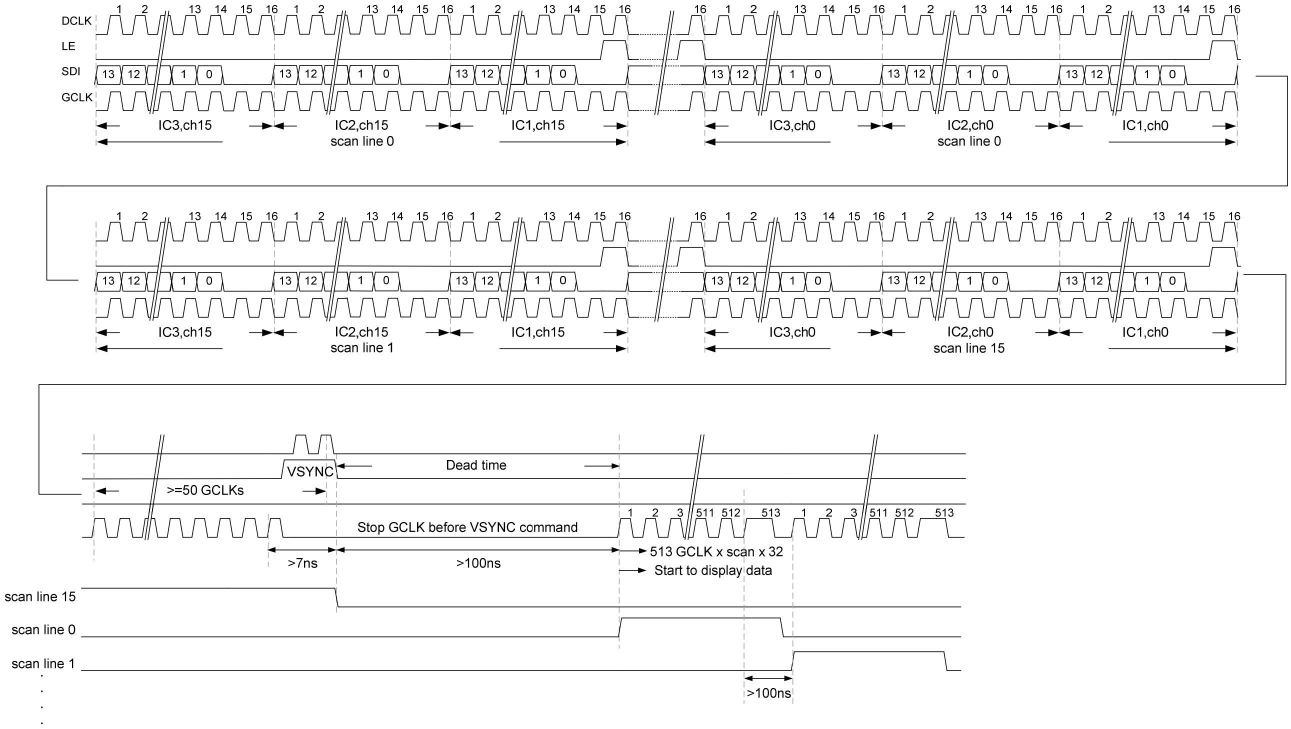

Figure 5. The timing diagram of 14-bit gray scale data

Section 3: Read configuration Register

The setting of read configuration register describes as below.

1. The command to read the configuration register 1 is LE arrested 5-DCLK rising edges, and LE arrested 90DCLK rising edges is to read the configuration register 2.
2. Configuration register data will be outputted from SDO, and each bit comes out with DCLK.
3. It needs16 x N of DCLK to send configuration register data, where N means the number of cascaded driver.
4. The read out sequence of cascaded IC is ICn→ ICn-1→…. →IC2→IC1.
5. The bit read out sequence is bit15→bit14→…. →bit1→bit0。
6. In the duration of read configuration, the SDI signal can be ignored.
7. Read out the configuration register data in non-display state is recommended.

Figure 6 shows the example of reading configuration register 1 in 3pcs cascaded MBI5152 .

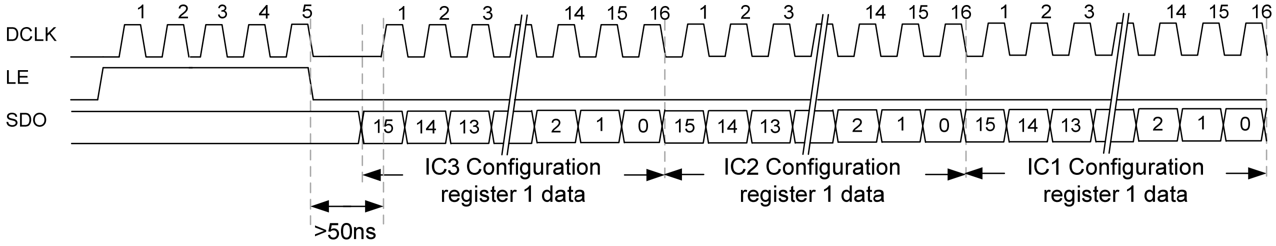
DCLK
LE
SDO
1 2 3 4 5
15 14 13 2 1 0
IC3 Configuration register 1 data
IC2 Configuration register 1 data
IC1 Configuration register 1 data
>50ns

Figure 6. Example of reading configuration register 1 in 3pcs cascaded MBI5152

Figure 7 shows the example of reading configuration register 2 in 3pcs cascaded MBI5152.

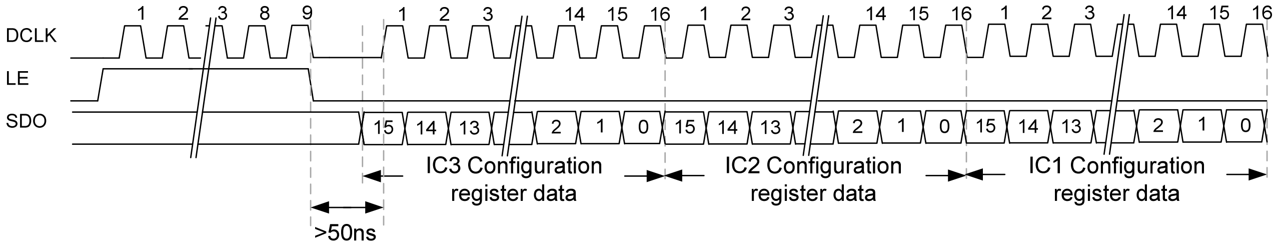
DCLK
LE
SDO
1
2
3
8
9
1
2
3
14
15
16
15
14
13
2
1
0
IC3 Configuration register data
IC2 Configuration register data
IC1 Configuration register data
>50ns

Figure 7. Example of reading configuration register 2 in 3pcs cascaded MBI5152

Section 4: Send Data and Display Image

MBI5152 embeds 8K-bit SRAM and divides it into two banks, SRAMA and SRAMB to reading and writing data frame. , SRAMB is used to play the current frame data, and SRAMA receives the gray scale data of next frame. After receive the Vsync command, the assignments of these two SRAM will be exchanged, as figure 8 shows.

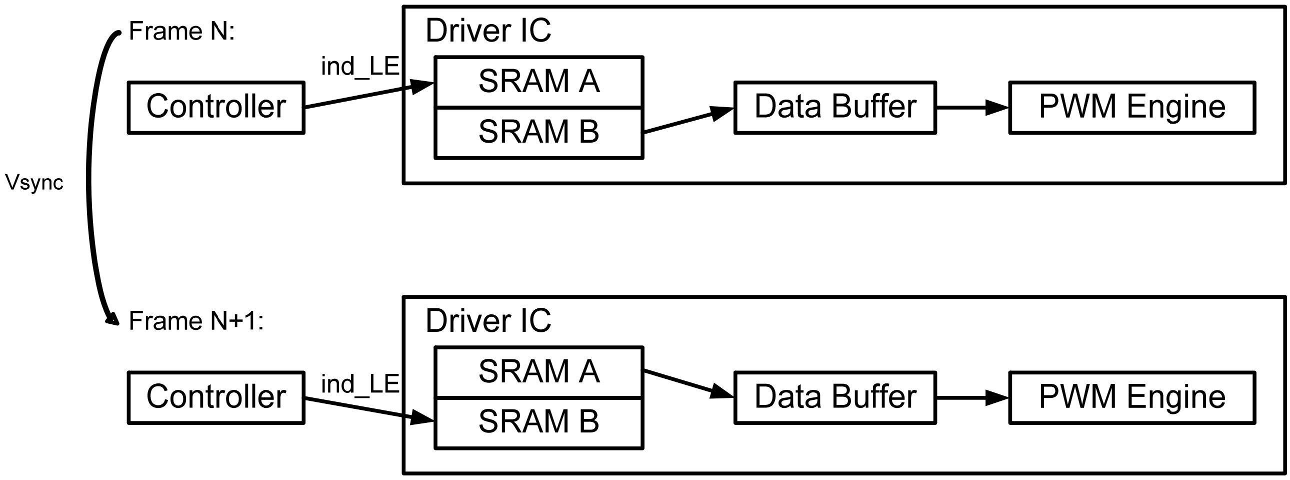

Figure 8. The data transmission structure of MBI5152

Section 5: Visual Refresh Rate and GCLK Multiplier Technology

Visual Refresh Rate

With S-PWM technology, the 16-bits PWM cycle of MBI5152 is divided into 64 sections, and each section has 1024 GCLKs. The 14-bits PWM cycle of MBI5152 is divided into 32 sections, and each section has 512 GCLKs. The formulas of visual refresh rate are

In 16-bits S-PWM mode, visual refresh rate $F_{visual} = \dfrac{1}{[1024\,x(1/F_{GCLK}) + t_{Dead}]\,x\,N}$ (1)

In 14-bits S-PWM mode, visual refresh rate $F_{visual} = \dfrac{1}{[512\,x(1/F_{GCLK}) + t_{Dead}]\,x\,N}$ (2)

where

F_{visual}: Visual Refresh Rate.

F_{GCLK}: Gray Scale Clock Frequency.

t_{Dead}: Dead Time.

N: Number of Scan Lines.

For example, for 16-bits PWM mode, the 1:16 time-multiplexing application with 15MHz GCLK frequency and the dead time is 10-GCLKs, the visual refresh rate could be calculated as below

$$F_{visual} = \frac{1}{[\,(1024+10)\,x(1/15MHz)\,]\,x\,16} = 906(Hz)$$

Since the frame data can be stored in the embedded SRAM of MBI5152, the updated data only need to complete transmission before next frame. The GCLK frequency needn't to follow the frame rate. If MBI5152's GCLK is 15MHz, the dead time is 10 GCLKs, table 3 shows the limitation of in each case.

Table 3. The limitation in different cases when GCLK=15MHz

Case	Bit numbers of gray scale control (bit)	Scan line	Frame rate (Hz)	Cycle number of GCLK counter in a period T_{DATA}
1	16	16	60	15
2	16	8	50	36
3	14	16	60	29
4	14	8	50	71

If the driver with 16-bits gray scale data, it needs 64 cycles to complete a frame data. That means both case 1 and 2 don't have enough time to complete a frame data transmission. Also, in 14-bits gray scale data, it needs only 32 cycles to complete a frame data. Case 3 doesn't have enough time to complete a frame data transmission. From above table, only case 4 can achieve this mission.

GCLK Multiplier Technology

If GCLK multiplier is enabled, GCLK will be dual edge triggered, that means the cycle time can be reduced by half, and the cycle number of GCLK counter in a period time will be double. Table 4 shows the results of GCLK multiplier enabled.

Table 4. The limitation in different cases when GCLK=15MHz (GCLK multiplier enabled)

Case	Bit numbers of gray scale control (bit)	Scan line	Frame rate (Hz)	Cycle number of GCLK counter in a period T_{DATA}
1	16	16	60	29
2	16	8	50	71
3	14	16	60	58
4	14	8	50	140

As MBI5152 GCLK multiplier is enabled, case 2, 3 and 4 can complete a frame transmission in 16-bits and 14-bits PWM mode respectively.

Take the 16-bit gray scale data for example, the Bits 15~7 are used to define the refresh rate (the SDI must larger than 64). The minimum output pulse width is the reciprocal of GCLK frequency.

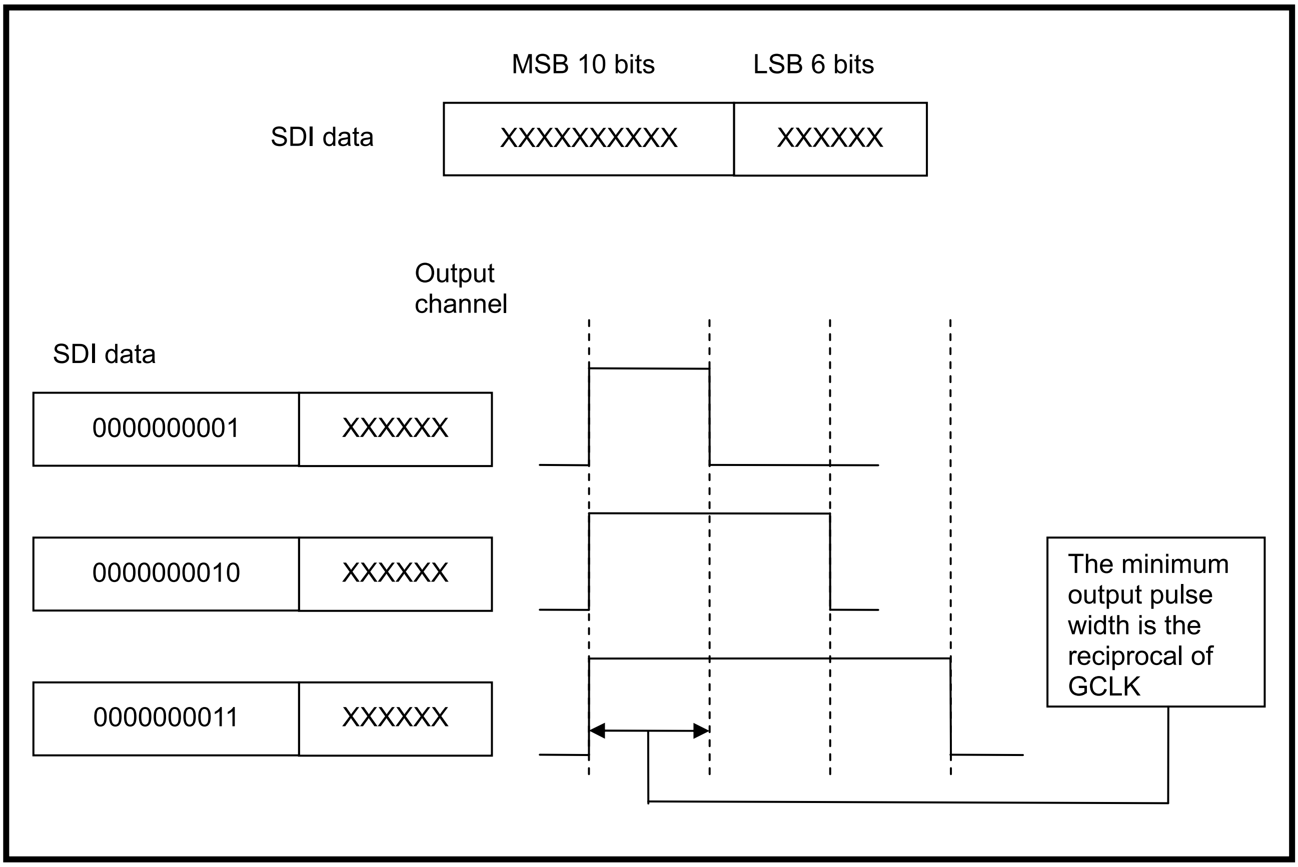

Figure 9. The diagram of SDI data and pulse width

Section 6: The Maximum Cascaded Number of MBI5152

The frame data must be updated in a picture period. Therefore, the maximum cascaded number of MBI5152 is decided by DCLK frequency and scan lines, and it can be calculated from the following equation

$$N = F_{DCLK} / (\text{the amount of data bit x scan line x frame rate}) \qquad (3)$$

Take the case 3 in table 5 for example, if the frame rate is 60 times/s, DCLK frequency is 15MHz, 1:16 time-multiplexing application, then from (3), the maximum cascaded number of MBI5152 is

$$N = (15\text{x}10^6) / [(16 \text{ x } 16) \text{ x } 16 \text{ x } 60] = 61$$

Table 5. The maximum cascaded number of MBI5152 at DCLK=15MHz

Case	Bit numbers of gray scale control (bit)	Frame rate (Hz)	Scan line	The maximum cascaded number
1	16	60	4	244
2	16	60	8	122
3	16	60	16	61
4	16	50	4	292
5	16	50	8	146
6	16	50	16	73

Section 7: Current Gain Adjustment

MBI5152 current gain can be adjusted from 12.5% (default) to 200%. No matter the output current is set by Rext or current gain, the adjusted current must keep in the constant current range of MBI5152. For example, after current gain adjustment, the output current must in the range of 1mA~20mA when V_{DD}=5.0V or 1mA~10mA when V_{DD}=3.3V. Otherwise, the over designed output current can't be guaranteed.

The Bit 5 to Bit 0 in configuration register 1 is used to set the current gain, and the defaulted gain code is 6'b101011. The Bit 5 is HC bit, HC=0 means in low current region, and HC=1 is high current region.

Table 6. The setting of current gain

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Define	-	-	-	-	-	-					HC	DA4	DA3	DA2	DA1	DA0
Default	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1

|← 6 bits current gain setting →|

The R_{ext} can be calculated by following equation

$R_{ext} = (V_{R\text{-}EXT} / I_{OUT}) \times 24$ .... (4)

where $V_{R\text{-}EXT}$ = 0.61Volt ×G, and G means the current gain.

The relationship of current gain (G) and gain data (D) is

HC=1, D=(65xG-33)/3 .... (5)

HC=0, D=(256xG-32)/3 .... (6)

Example 1

If I_{OUT} =10mA and G=1, then the gain code is

Step 1: From (4), the R_{ext} = [(0.61 × 1) / 10mA] × 24 = 1464Ω. From figure 10, G=1 in the high gain region, that means the HC=1. Thus, substitute above information into (5), the D=(65xG-33)/3=10.67≒11.

Step 2: Convert D into binary, D=01011, therefore DA[4:0]= 01011.

The 6 bits (bit 5~bit 0) of the configuration register are 6'b101011.

Example 2

If R_{ext} is 1464Ω, the adjusted output current is from 10mA to 18mA, then

Step 1: G= 18mA /10mA =1.8 (HC=1).

Step 2: From (5), D= (65x1.8-33)/3=28.

Step 3: Convert D into binary, D=11100, therefore DA[4:0]= 5'b11100.

Step 4: The adjusted gain code is 6'b111100.

Example 3

If R_{ext} is 1464Ω, the adjusted output current is from 10mA to 3mA, then

Step 1: G= 3mA /10mA =0.3 (HC=0).

Step 2: From (6), D= (256x0.3-32)/3=14.9≒ 15.

Step 3: Convert D into binary, D=01111, therefore DA[4:0]= 5’b01111.

Step 4: The adjusted gain code is 6’b001111.

Figure 10 shows the relationship of current gain and gain code. The defaulted gain code of MBI5152 is 6’b101011, is corresponding to 1.015 current gain.

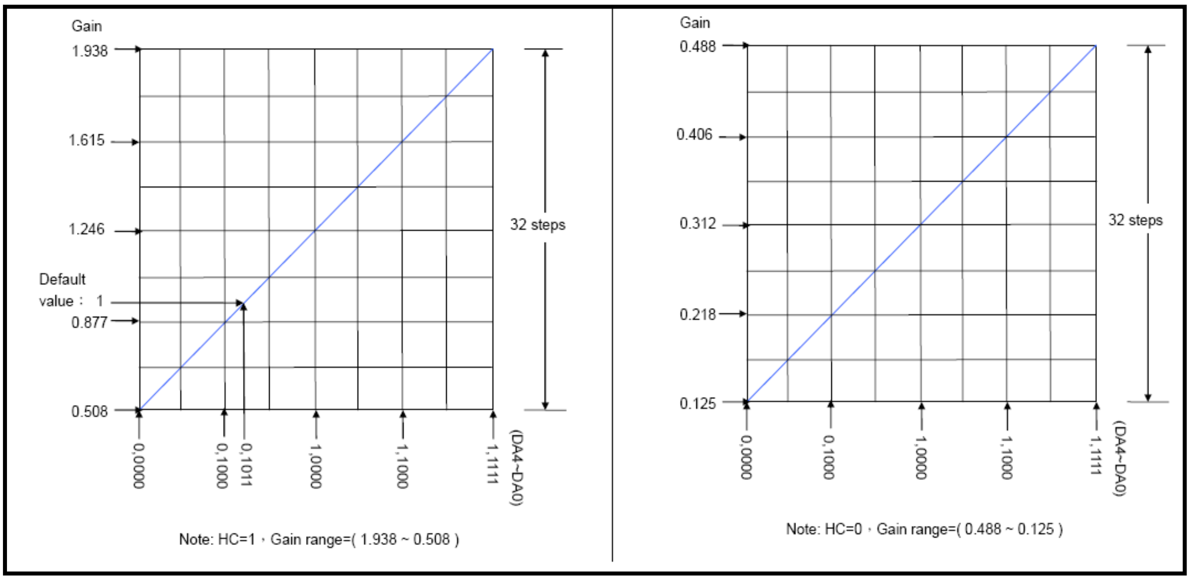

Figure 10. The relationship of current gain and gain code

Figure 11 is the relationship of output current and gain data under V_{DD}=5.0V and R_{ext}=1400Ω. The defaulted current gain, G =1, is corresponding to 10mA.

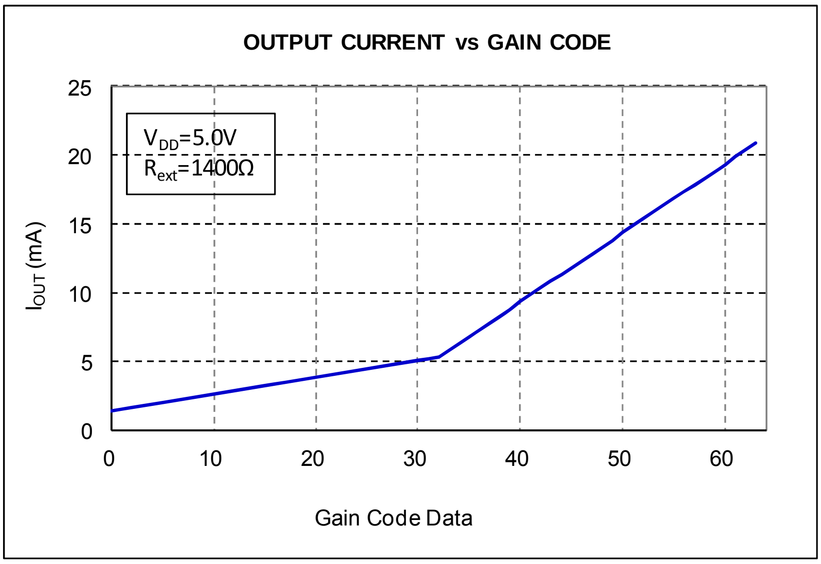

Figure 11. The relationship of output current and gain code at 5.0V, Rext=1400Ω.

Section 8: The Notice of LED Open-Circuit Error Detection

As figure 12 shows, MBI5152 executes the compulsory open-circuit detection while the LE high pulse is sampled by 7-DCLK rising edges. In the duration of compulsory open circuit detection, all the output channels will be turned off.

When LE high pulse pin is sampled by 1-DCLK rising edge, the result of open circuit detection will be shifted out from the SDO pin and the sequence is from MSB to LSB. The error detection will stop while the result is shifted out.

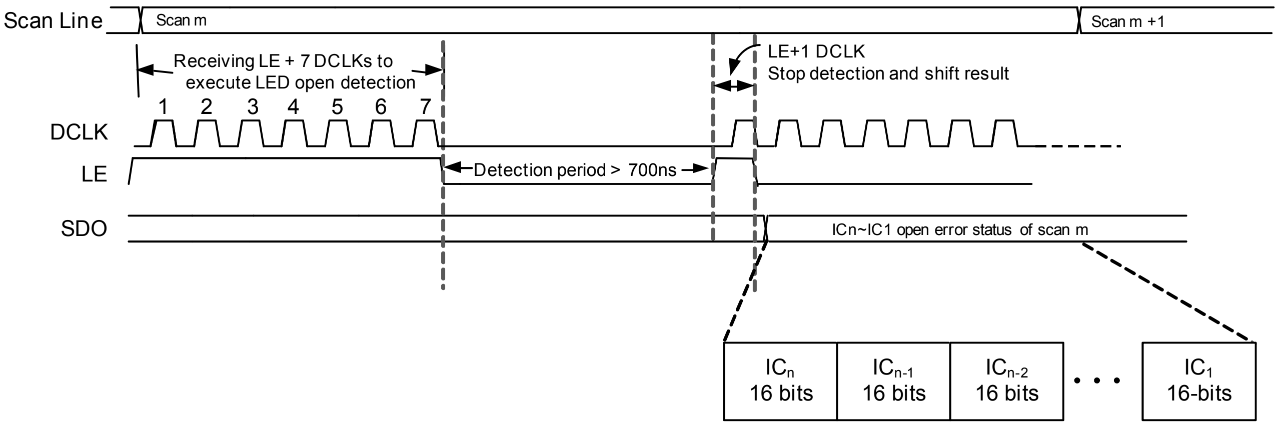

Figure 12. The timing diagram of compulsory open-circuit detection

In the duration of compulsory open-circuit detection, the SDI data can be ignored. In addition, the following notices must be taken

1. During the detection, the frame cannot display normal until LE arrested 1-DCLK rising edge. The duration should be keep longer than 700ns, as figure 12 shows.
2. When output turns on, please make sure the output voltage (V_{DS}) is higher than 0.3V. The bit [9:8] in configuration register 2 can choose open-circuit detection voltage by 0.3V/0.4V/0.5V/0.6V.
3. In the duration of compulsory open circuit detection, the scan line can’t switch.
4. MBI5152 doesn't support LED short circuit detection.

Table 7. Error code

Status	Detected Result
Open	0
Normal	1

Section 9: Ghost Elimination in the Time-Multiplexing LED Displays

There are two types of ghosting problems in time-multiplexing application

1. The phenomenon of unexpected LED in last scan line slightly turns on called “upper ghost problem”. Please refer the follow method to prevent it.

Figure 13 is an example of time-multiplexing application with n-scan lines. To avoid the upper ghost problem, the discharged circuit between the V_{LED} and GND of each scan line is recommended. Typically, the discharged circuit is a resistor cascaded with a zener diode. The resistance is about 390Ω~1kΩ, and the zener diode is about 3.0~3.3V, it can be adjusted based on the actual condition.

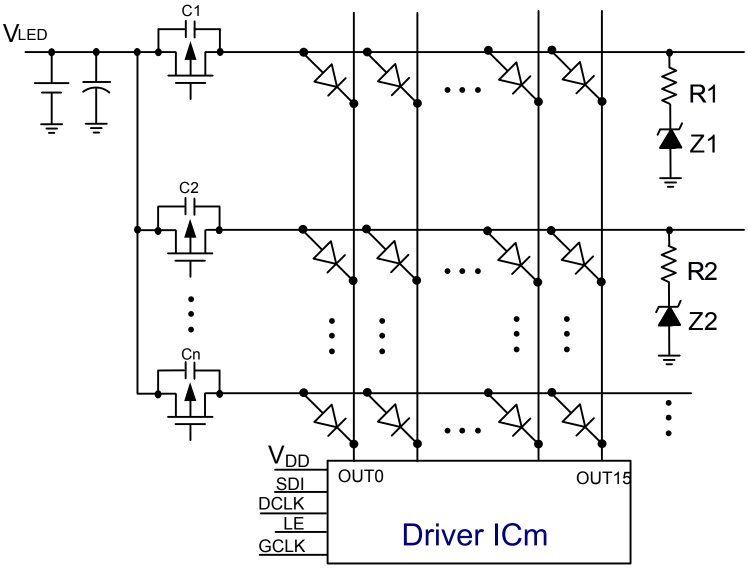

Figure 13. Circuit diagram of upper ghost elimination

2. The phenomenon of unexpected LED in next scan line slightly turns on called “lower ghost problem”.

The bit[F] of configuration register1 is used to enable the lower ghost elimination, and figure 14 shows the timing diagram. In the dead time, the duration between the falling edge of 1025th GCLK and scan line switched determines the running time of lower ghost elimination.

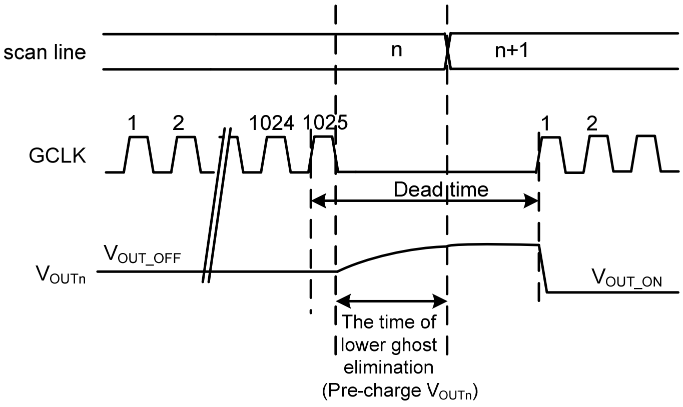

Figure 14. Timing diagram of lower ghost elimination

Figure 15 shows the display example with diagonal line pattern, the ghost problem is apparent, and figure 16 shows the improvement which has enabled the lower ghost elimination.

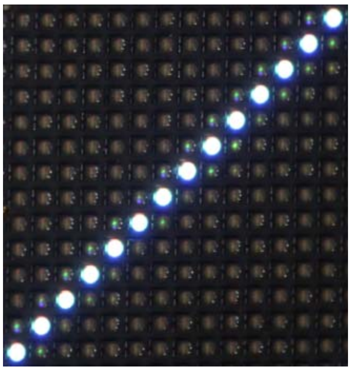

Figure 15. Display board with ghost problem

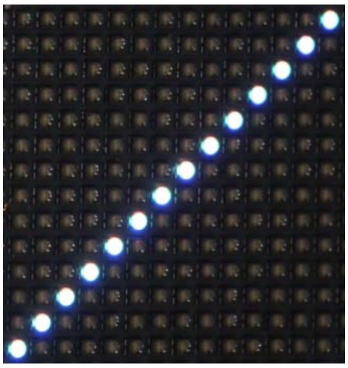

Figure 16. The display board with ghost elimination function

Enhance Mode of Lower Ghost Elimination

Not only enable lower ghost elimination can improve the lower ghost phenomenon, MBI5152 also provides enhance mode to eliminate the lower ghost phenomenon. De-ghost function must be enabled first, and then set the enhance mode according to the different loading, as table 8 shows.

Table 8. The setting table of enhance mode to eliminate the lower ghost

Configuration register 1 bit[F]	Configuration register 2 bit[D,C]	Comment
1	00、01(default)	Suitable for Red LED
1	10	Suitable for Green LED
1	11	Suitable for Blue LED

Section 10: Improve the Dim Line Problem

In the time-multiplexing application, the parasitic capacitance exists in PCB layout trace, and is inconsistent in display board. The dim line problem is the most common problem in LED display, as figure 17 shows.

To improve this problem, the bit[3:1] in configuration register 2 is used to extend the output on-time. Figure 18 shows the improvement.

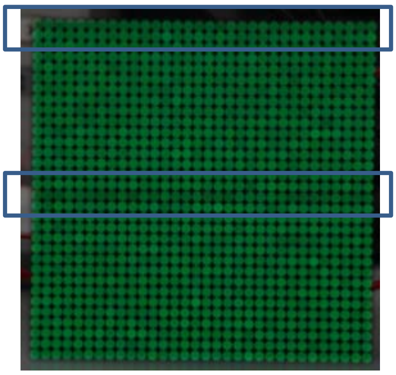

Figure 17. In 1:16 time multiplexing application, Green LED has dim line problem.

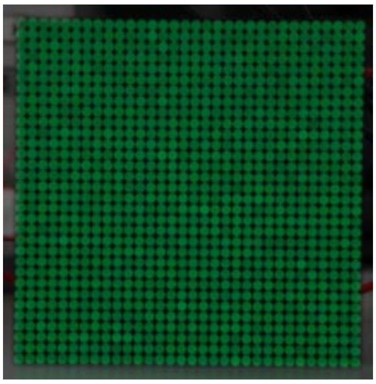

Figure 18. The Green LED dim line problem has been improved as configuration register 2 bit[3:1] set [100]: 18ns.

To extend the output on-time, there is one thing must be taken, the extended time can't longer than 1/2 of GCLK period, otherwise, the extend function will be invalid. For example, if the GCLK frequency is 20MHz, and the period time of GCLK (T_{GCLK}) is 50ns, then the extended output on-time can't longer than 25ns.

Section 11: Software Reset

When the software reset command is enabled, the internal counters of GCLK and data latch will be reset, and turned off all the output channels. However, the gray scale data stored in the SRAM, configuration register and current gain won't be reset.

Summary

MBI5152 uses the embedded S-PWM to control LED current and provides a storage solution of 8K-bit SRAM. Users don't need to send new data every time. This article provides the design guideline for uses.